Advanced V-LINK DDR Platform Architecture

February, 2001
Platform Conference

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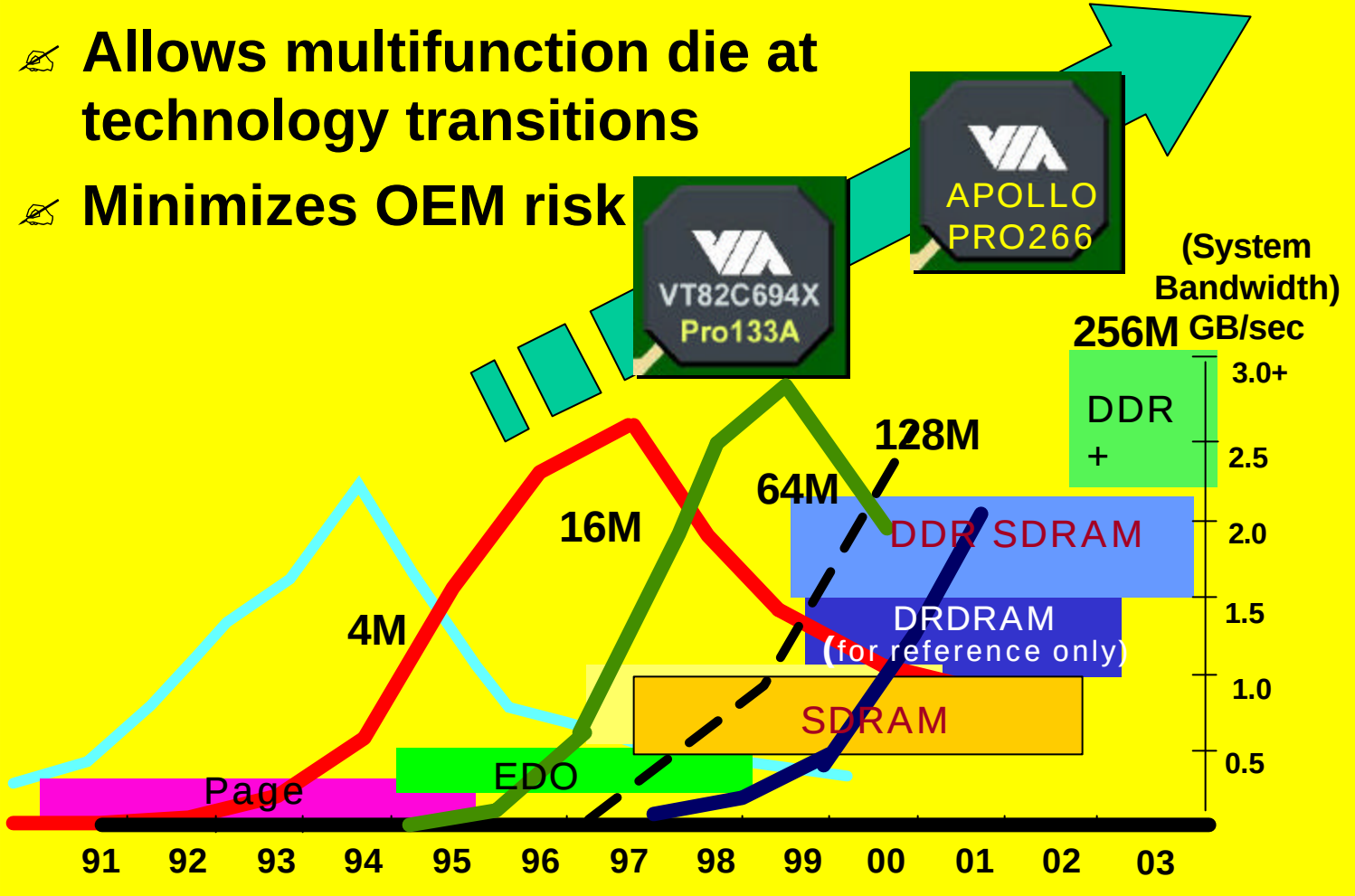
Senior Director, Product Marketing

Agenda

- DRAM Evolutionary Path
- Hi-Perf. DDR North Bridge Features
  - VT8633, Pro266
  - VT8366, KT266
- Highly Integrated V-Link South Bridge Features - VT8233
- ACR, the STD for Networked PC
- DDR Promotion/Enabling Program
- Summary

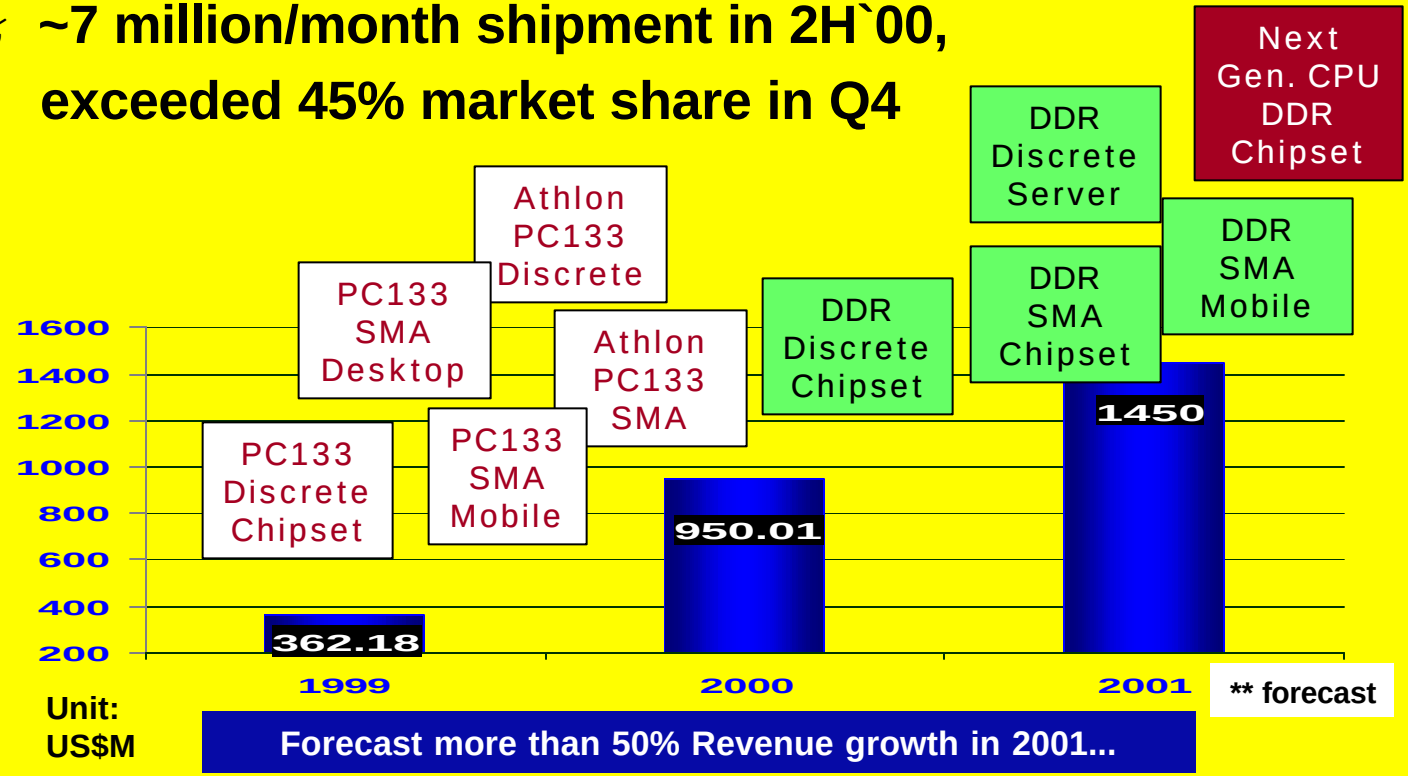
“DRAM Evolutionary Path”

- Maximizes infrastructure reuse
- Minimizes costs
- Allows multifunction die at technology transitions
- Minimizes OEM risk



VIA: Market Position

- Full System Logic Product Offering from Performance to Value segments
- Incremental, Smooth migration with Pin/driver compatibility
- Modular design and fast execution
- ~7 million/month shipment in 2H`00, exceeded 45% market share in Q4



DDR SDRAM the next PC mainstream memory

- DDR SDRAM suitable for every market segment
  - x86 and RISC-based Server
  - Hi-perf. Desktop PC and Workstation
  - Mainstream Desktop and SMA value PC
  - Low Power Mobile applications
- DDR SDRAM utilizes existing SDRAM experience
- DDR SDRAM is an open standard
- DDR SDRAM has superior architecture than SDR SDRAM
  - Double data transfer rate per CLK
  - Source Synchronize reduce signal flight time skew

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VIA DDR Chipset Strategies

- Enable System OEMs and System Integrators to build the highest performance DDR SDRAM based desktop & mobile PCs for both Pentium and Athlon™ Processors in 1H`01
- Drive and expand DDR application to Server/Workstation, SMA Value Desktop and Mobile markets in 2H`01
- Establish a Networking ready platform with industry standard Advanced Communication Raise Slot (ACR)

VIA Apollo DDR Chipset Highlights

- **High performance DDR North Bridge:**
  - **Pro266: PentiumIII socket-370 FSB 100/133MHz**
  - **KT266: Athlon Socket-A FSB 200/266MHz**
  - **DDR200/266 and PC100/133 System Memory of up to 4GByte**
  - **AGP port Interface 2X/4X modes**
  - **V-Link Hub architecture with 266MB/s bandwidth to replace PCI bus**
- **Highly Integrated Networking Ready South Bridge VT8233**
  - **V-LINK 266MB/S to North Bridge**
  - **Support 6 slots PCI bus system expansion**
  - **Dual ATA100/66/33**
  - **6 USB ports, USB 1.1 compliant**
  - **Integrated Networking MAC with external PHY for 10/100Mb Ethernet or Home PNA**
  - **Advanced 6-channel Audio and HSP Modem**
  - **LPC to replace ISA bus**
  - **PMM: ACPI & OnNOW, PowerNow™**

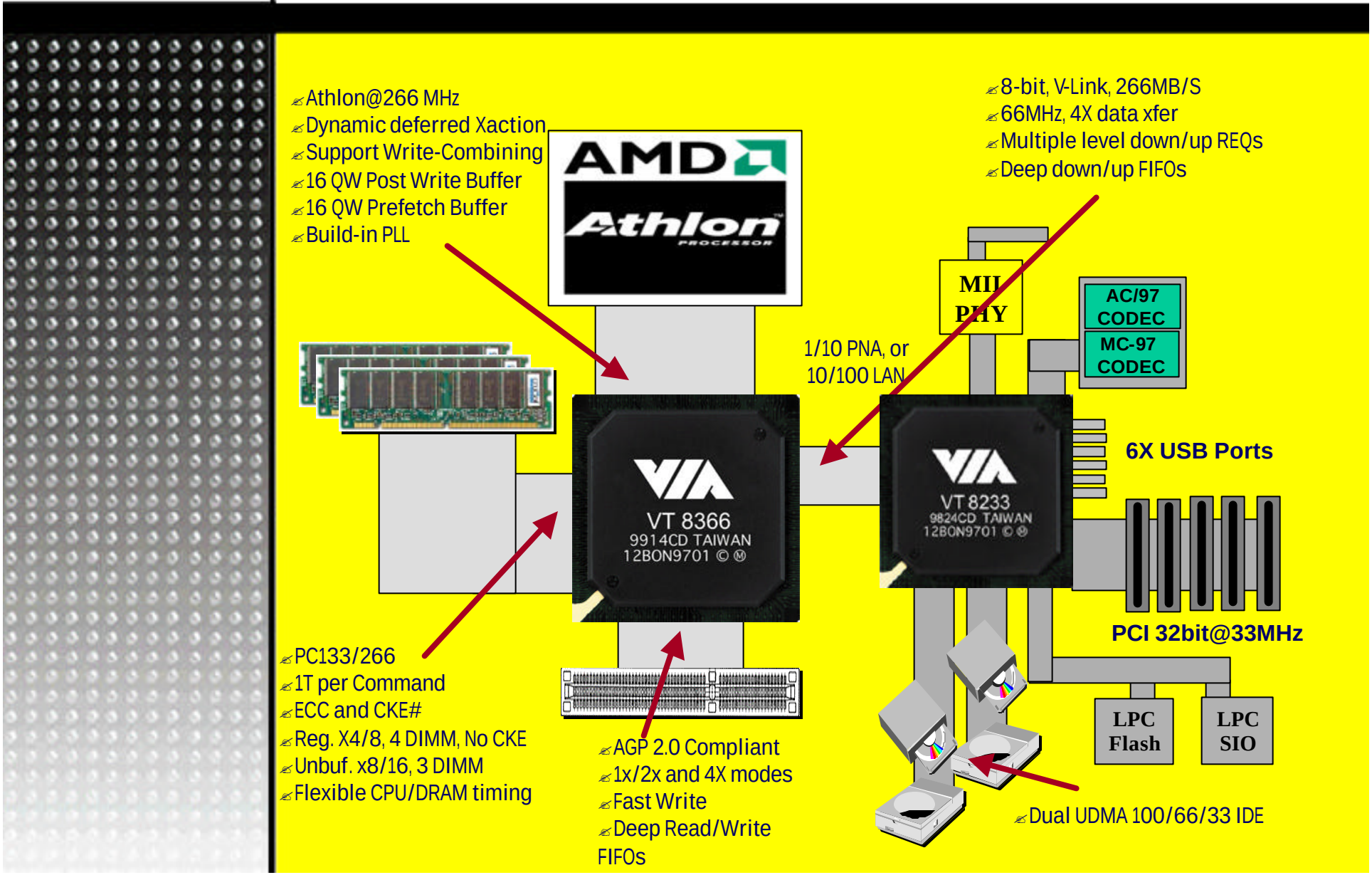
KT266

- FSB 200/266MHz
- DDR200/266SDRAM
- AGP Port Interface
- V-LINK 266MB/S

VT8233

- ATA33/66100
- 6 USB ports
- Networking ready
- Int. Audio, SW Modem

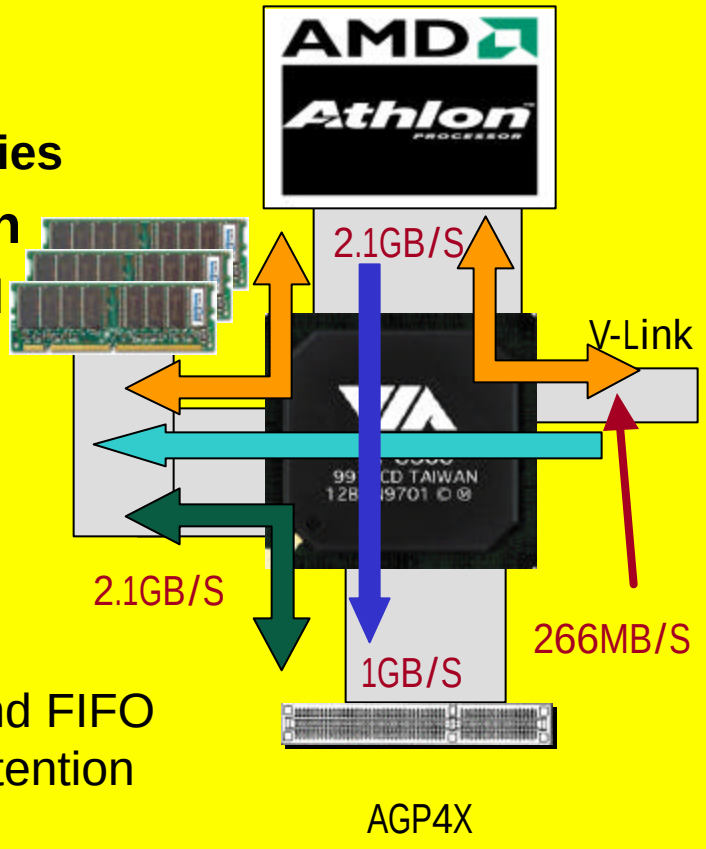
Apollo KT266 V-Link Athlon DDR Chipset System Partition



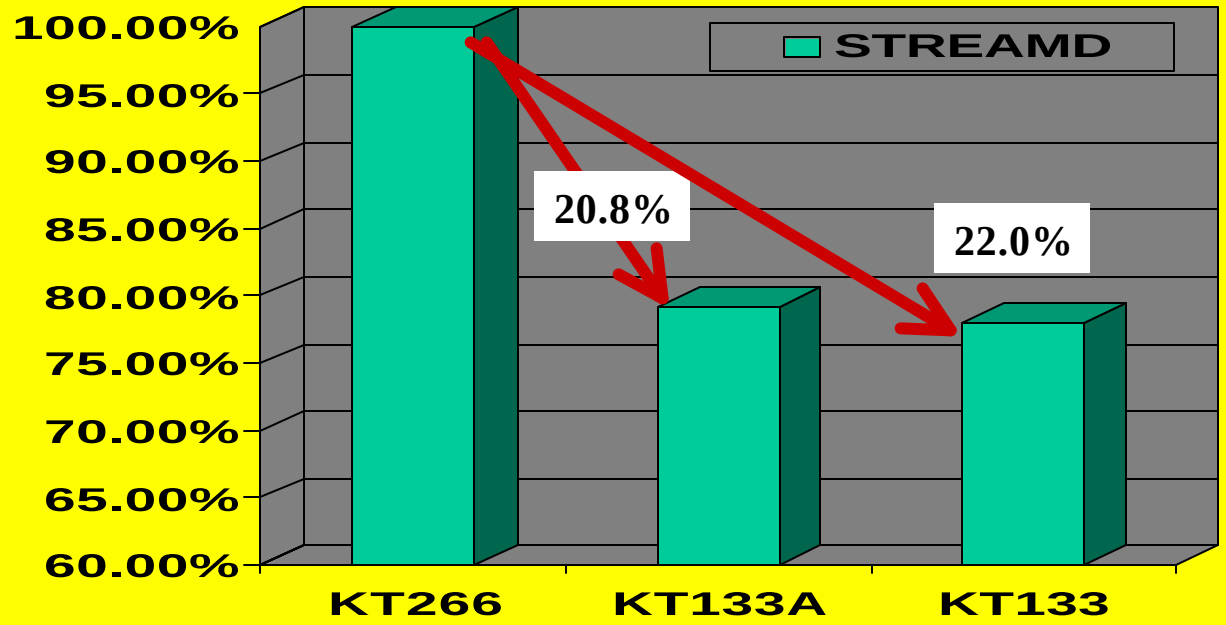
VIA Apollo DDR Chipset Streamline System Data Traffics

Latency, CMD & Data Xfer/per CLK, Data Trashing, etc ....

- **Well balanced system bandwidth**
  - **Peak-peak bandwidth**
  - **Cycle-cycle latency**
  - **Sync/Async Buses frequencies**
- **Improve bandwidth utilization**
  - Improve CPU-DRAM front-end access latency - 1T per CMD
  - Out-of-Order data access improve utilization rate
    - Read-around-Write
    - Write-Combines
  - intelligent DRAM arbitration and FIFO management reduce data contention
  - And more...



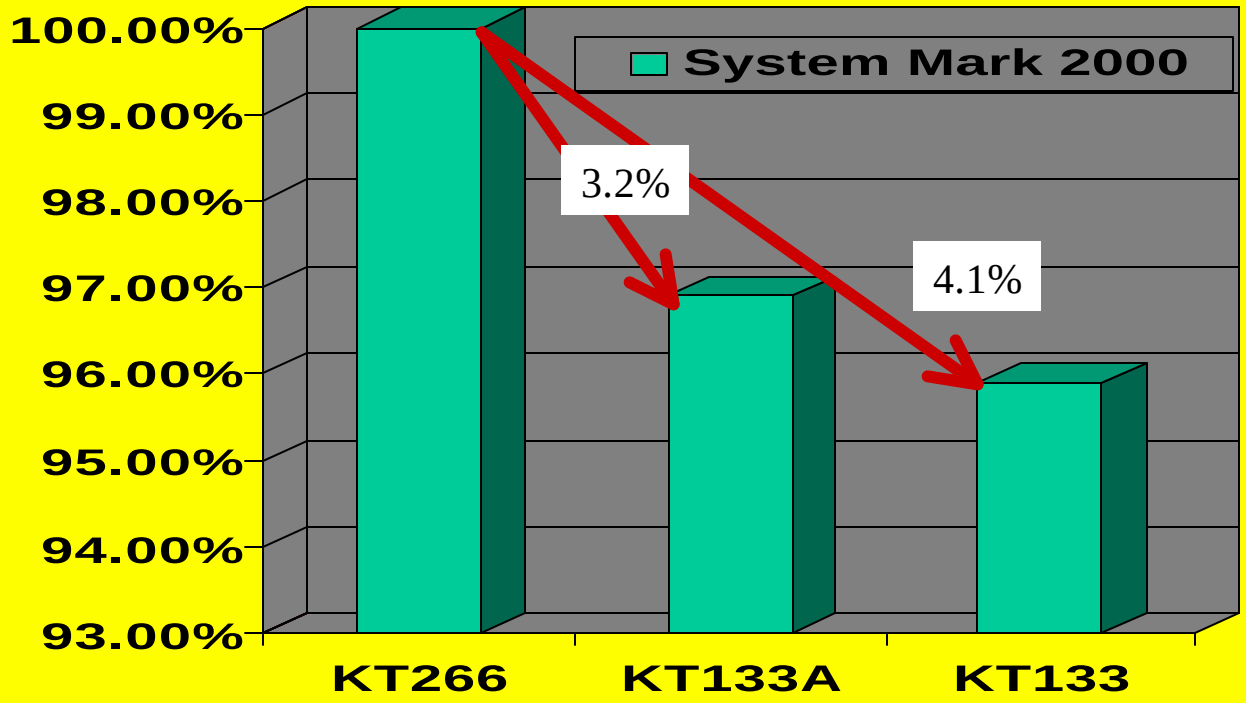
Apollo DDR SDRAM Double Memory Subsystem Bandwidth



- **STREAMD is a DRAM subsystem performance stress benchmark**
  - **It is widely used in Server, Workstation applications**
  - **It is a good indicator of Memory performance and memory bandwidth headroom**

Common System Configuration: Win98, SE. 1GHz AthIon, 128MB DRAM, ASUS V7700 NV15 Graphics card, IBM DTLA307030 ATA100 HDisk
1. KT266 System: FSB266, DDR266; 2. KT133A System: 266FSB. PC133; 3. KT133 System: FSB200, PC133.

Apollo KT266 System Mark 2000



- System Mark 2000 is CPU intensive Benchmark
  - Latency is more critical to the System Mark 2000, but
  - System do benefit of higher memory bandwidth

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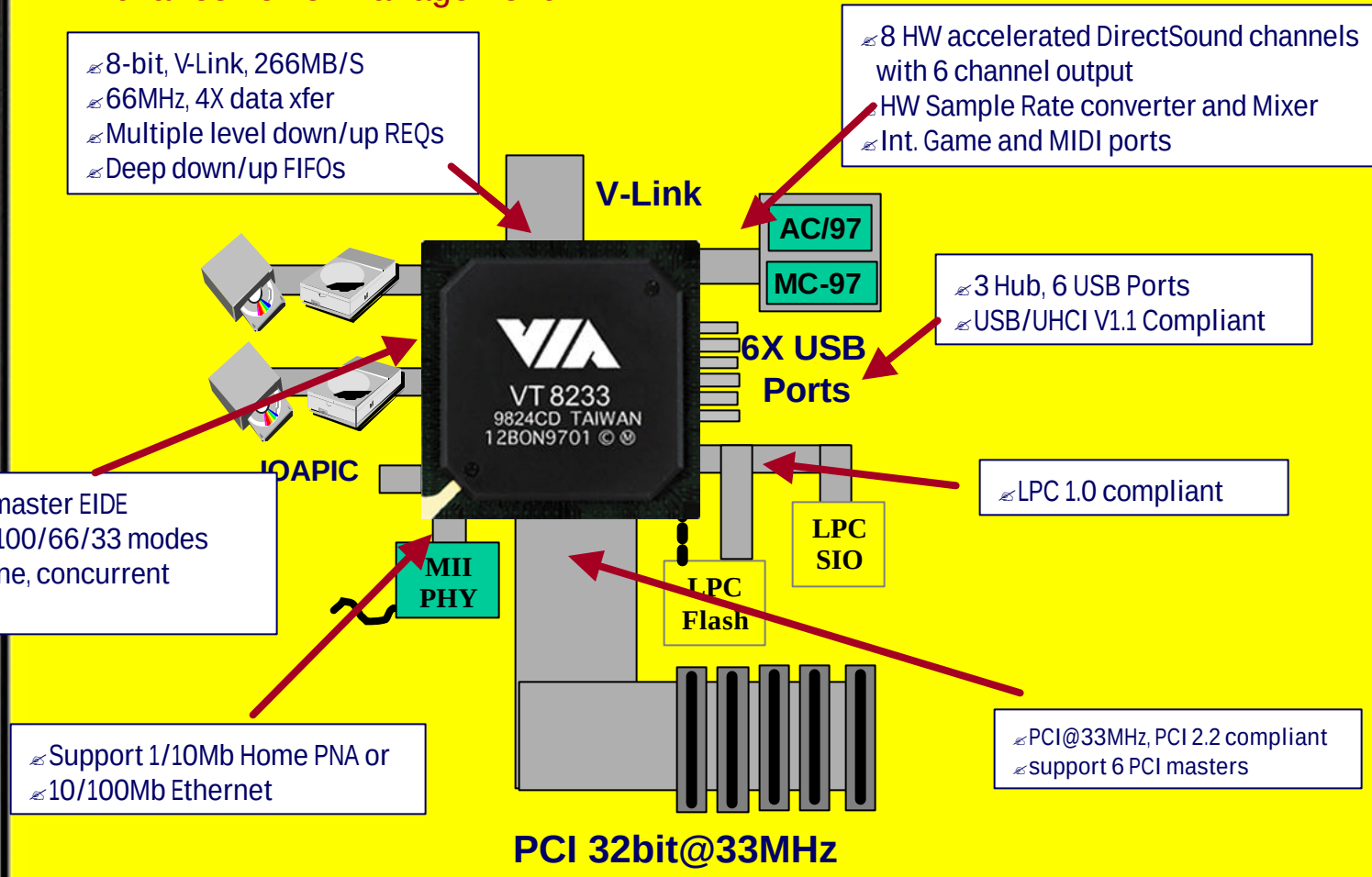
Apollo Highly Integrated VT8233 V-Link Networking Ready LPC South Bridge

- V-Link SB, double N/S bandwidth to 266MB/S
- Highly integrated, PC99 compliant legacy free south bridge
- Advance Power Management



32-bit/33MHz PCI bus issue

Unbalanced System when pairing with DDR North Bridge

- **Low Utilization rate**
  - **PCI bus arbitration, Address/data mux., Turn-around penalty, etc...**
- **Highly integrated South Bridge saturates 32-bit 33MHz PCI bus**
  - **Dual ATA100 IDE channels, Networking, Multi-USB ports, Digital audio/modem**
  - **Slow down overall system performance, especially for a value system with less DRAM**

V-LINK Hi-Speed PTP Interconnect Technology

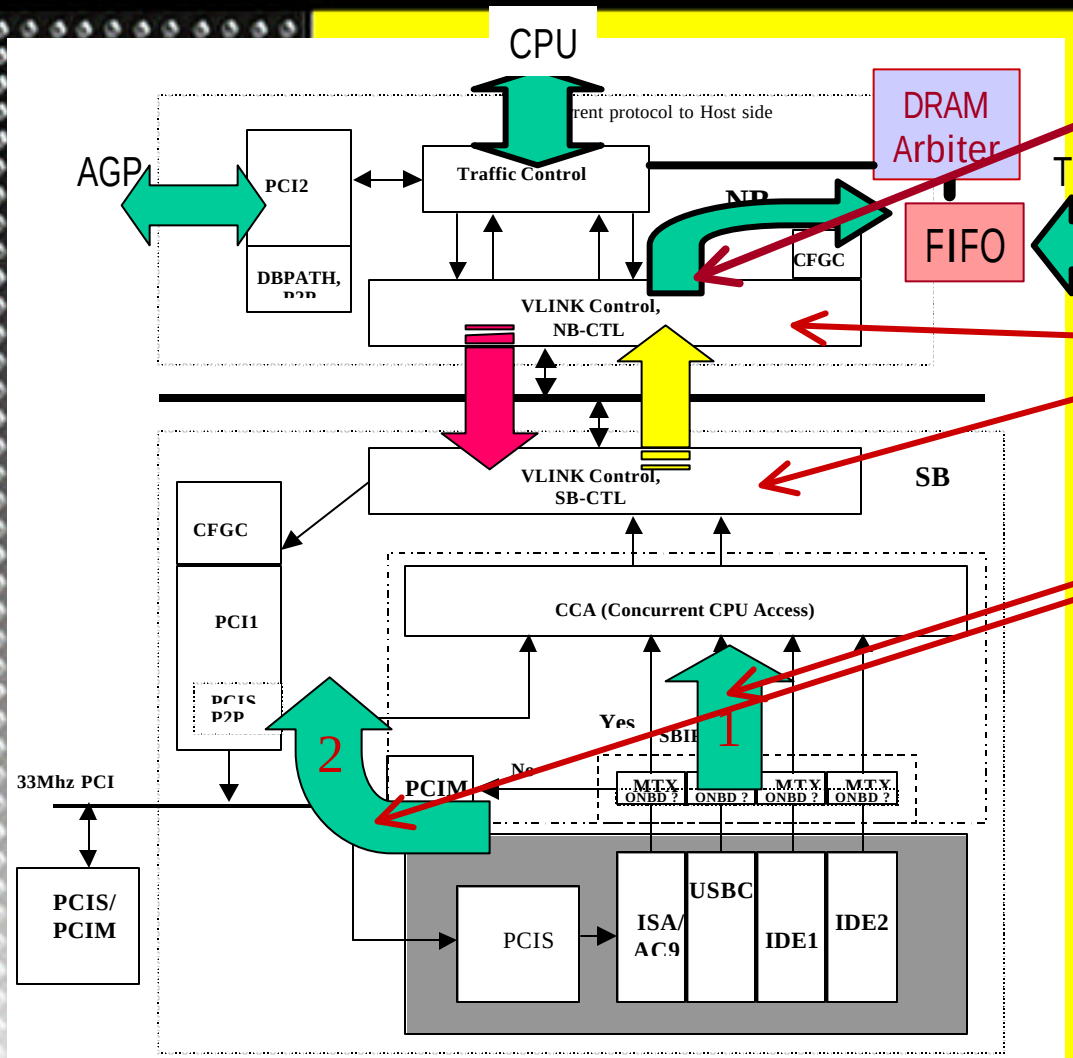


Figure 1. System logic block diagram

North Bridge

- Extension of NB Memory Bus
- Low Latency, High Efficiency
- Support System data coherence

V-LINK Bus Highlights

- SW transparent
- 8-bit, 2X/4X operation @66MHz Bus
- Full Duplex of up/down CMD/Data streams
- REQ/DATA split transaction
- Multi-Levels Up/Down stream Queue

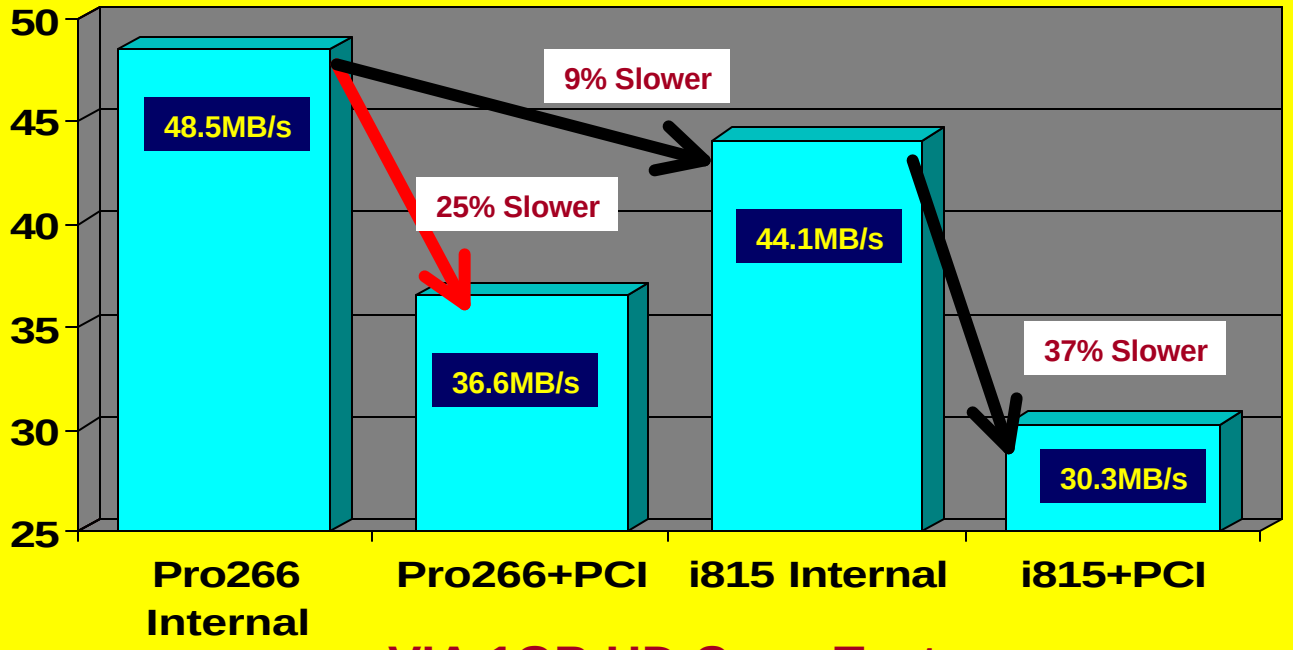
SB internal Bus:

- Concurrent Dual Request/Data paths for integrated functional blocks
- 66MHz PCI bus
- 100% backward compatible

V-Link Benefits:

- SW Transparent & Low pin count
- Double bandwidth vs PCI 33/32
- More headroom for future expansion
- Low latency, high efficiency

V-Link Double NB/SB Bandwidth



VIA 1GB HD Copy Test

- A Extension of North Bridge internal Memory bus
- Peak bandwidth of 266MB/S with low latency and reduce bus arbitration and turn-around penalty
- Multiple mechanisms to configure priority
- Technology allows speed up to 533MB/S in 2H/01

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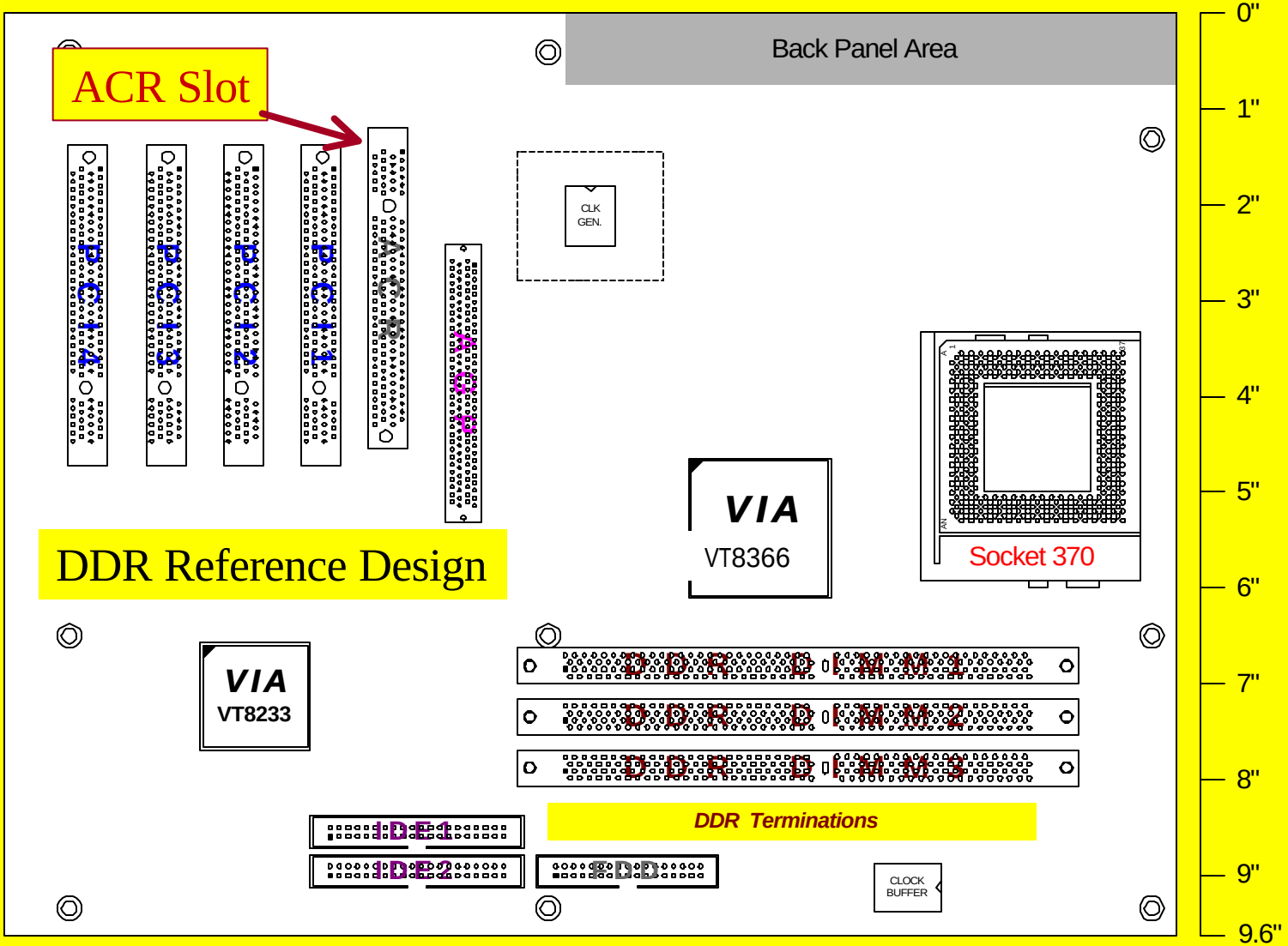
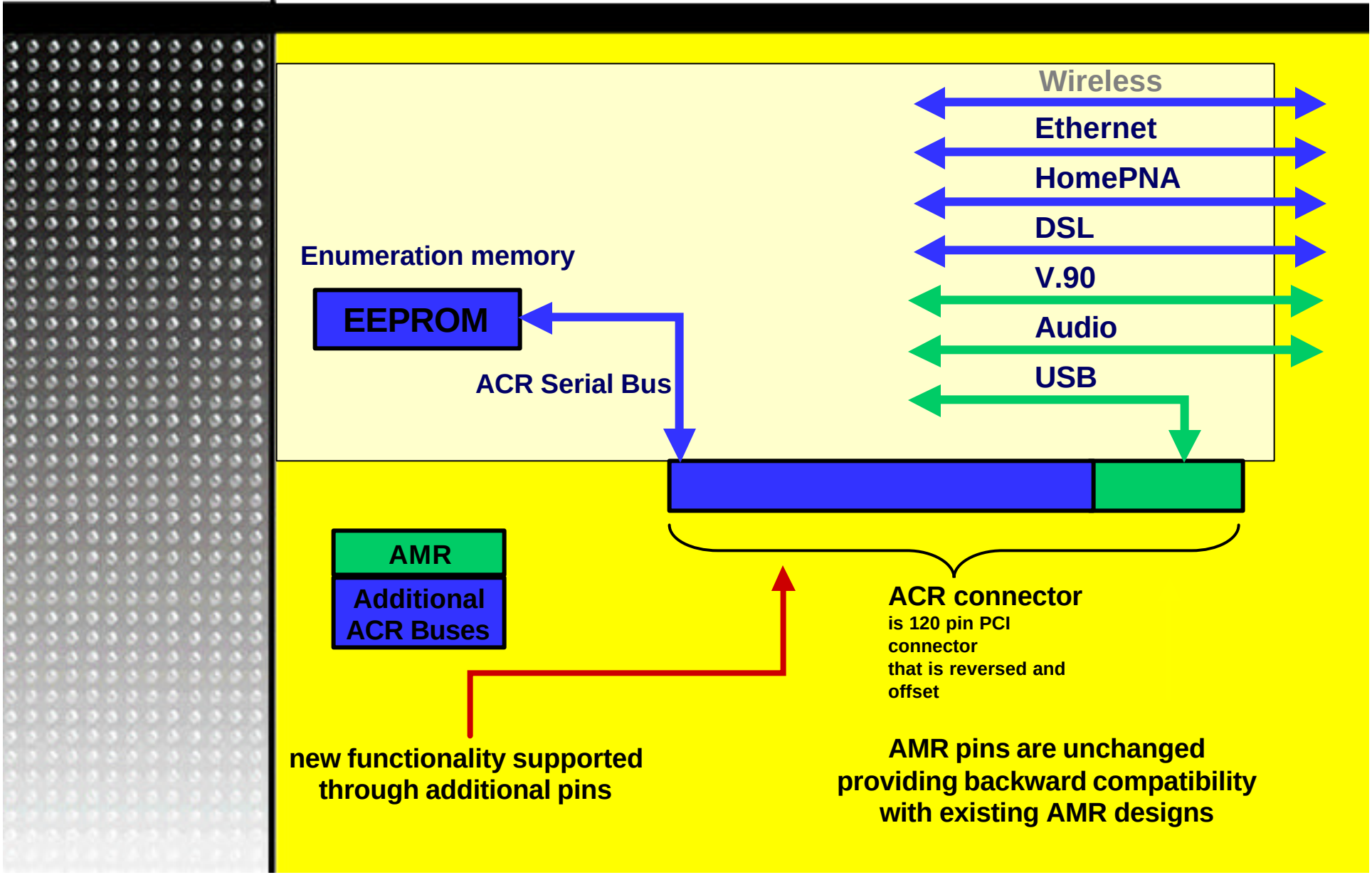
DDR MB Design Reference



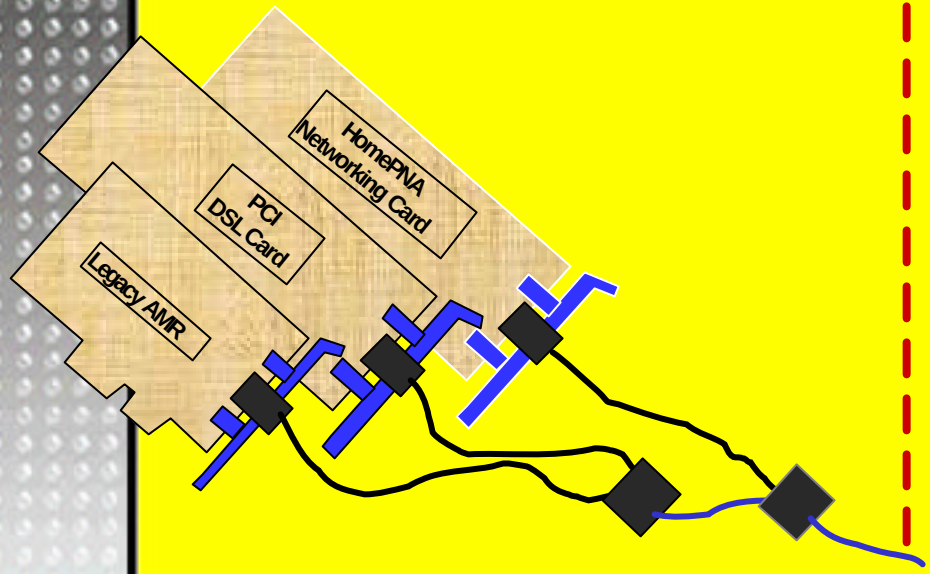
ACR Concept Diagram

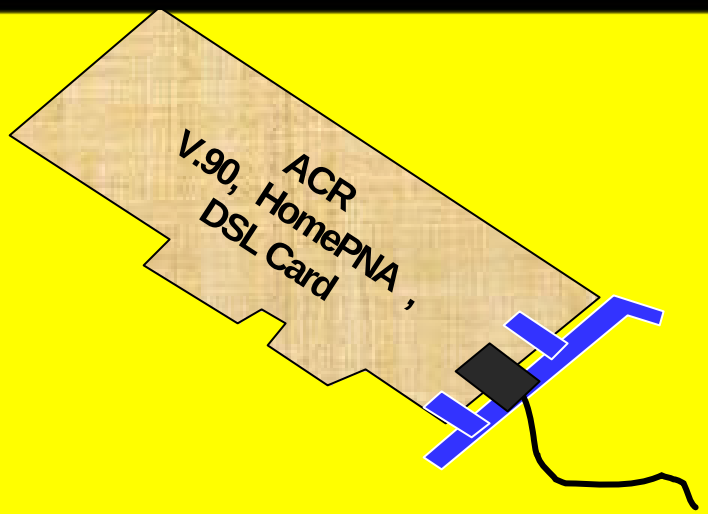


Simplifies RJ11 connections

Legacy Designs

- Need separate cards for each phone line function and require adapters to merge the lines into one combined phone wire





ACR Designs

- Combine all the phone line functions on a single card that uses a single RJ-11 connector

Possible Configurations Today

Residential Client

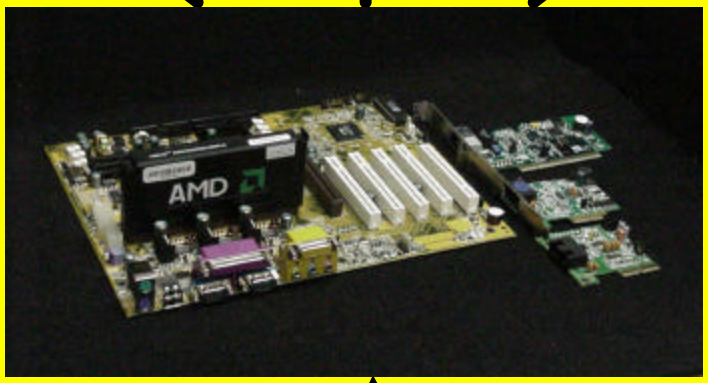
- V.90
- 10/100 base-T
- HomePNA 1,2
- 2 Ch audio

Desktop

- V.90
- 2 Ch audio

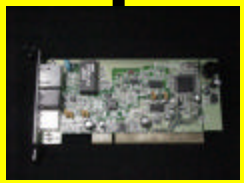
Residential Gateway

- V.90
- 10/100 base-T
- HomePNA 1,2
- DSL(in layout)
- Cable(Ethernet)
- Multi-Channel Audio



ACR motherboards

VIA ACR.Lite & ACR.Hub



ACR Riser Cards

ACR.Basic, ACR.Lite, ACR.Hub

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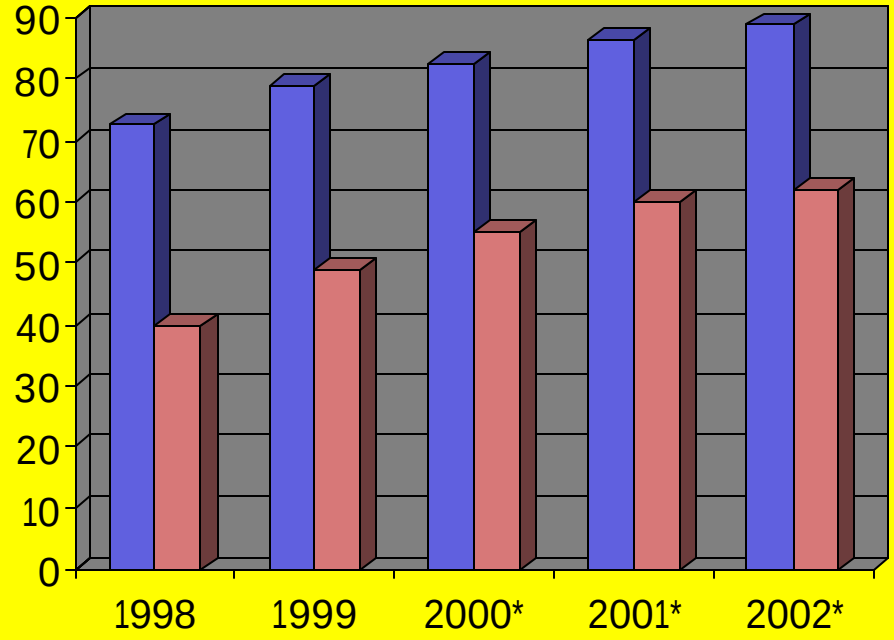
DDR Promotion/Enabling Program

- **Much tougher task than PC133**
  - New MB design, Diff. DRAM interface, New parts
- **VIA plays key role to drive the market demand**
  - DDR Validation Program in place with Smart Module and CMTL
    - 8 top tiers' DDR modules had passed validation (Jan. 08)
  - Design-Wins with leading MB/System OEMs (Jan.08)
    - Pro266: 43 Design-wins
    - KT266: 22 Design-wins
  - MP DDR chipsets to create demand of DDR modules
  - Drive APAC MB mfr. Engine to lead the market trend
  - Drive DDR readiness of MB/Sys infrastructure to prepare for quick ramp of OEM market

DDR Enabling: Prepare APAC DDR-based MB/System Infrastructure

- **Accelerate DDR chipset development**
- **Continue drive DDR design-wins**
  - **To establish DDR turnkey solutions infrastructure**

Market Share%



MB/System and Mobile PC that manufactured in Taiwan and PRC worldwide Market Share

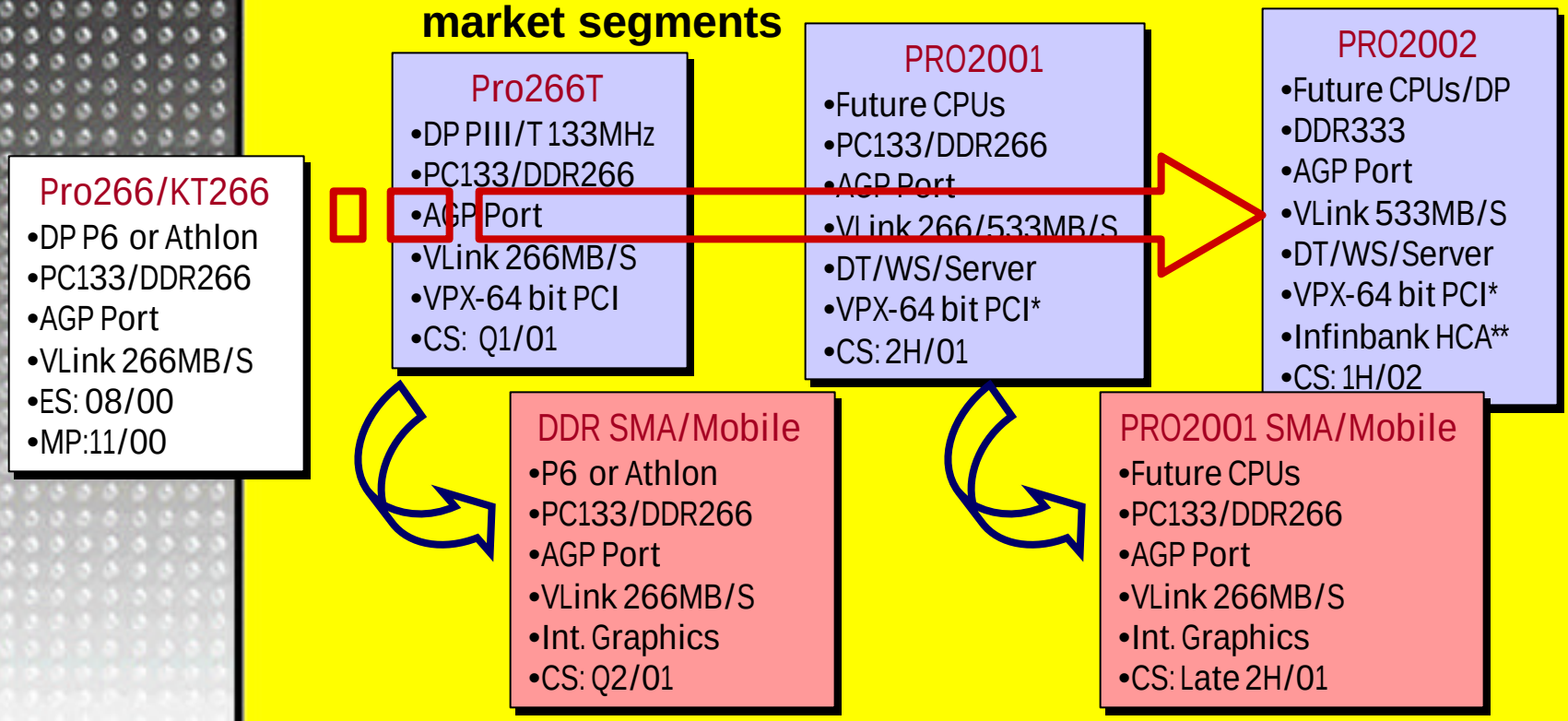
- **MB and System Integrator are the leading PC trendsetter**
- **More and more OEMs goes to APAC for the Off-the Shelf products for Time-to-market and lower product cost**
- **Enabling APAC manufacturers infrastructure is key to secure OEM business**

DDR Promotion Events:

- **Objectives:**
  - **To max. DDR media coverage and DDR awareness**
  - **Enhanced DDR market momentum**
  - **To re-assure MB makers and System Integrators of DDR pricing and availability**
- **Events:**
  - **DDR Summit Press Conference & Pavilion**
    - **Feb. 06, 2001, Taipei, TICC**
  - **VIA DDR MB Media Evaluation Rebate Promotion**
    - **Provide a rebate program to encourage MB/SI/OEMs to submit DDR system to media for evaluation**
    - **Generate market awareness and stimulate demand**
    - **71 medias and across 16 countries**

VIA DDR chipset Roadmap

- **Advanced VIA Apollo DDR chipset architecture**
  - **Superior performance, eliminate system bottleneck**
  - **Fully validated, one generation ahead of competitors**
  - **Scalable architecture with plenty bandwidth headroom**
  - **Compelling cost structure and suitable for all PC market segments**



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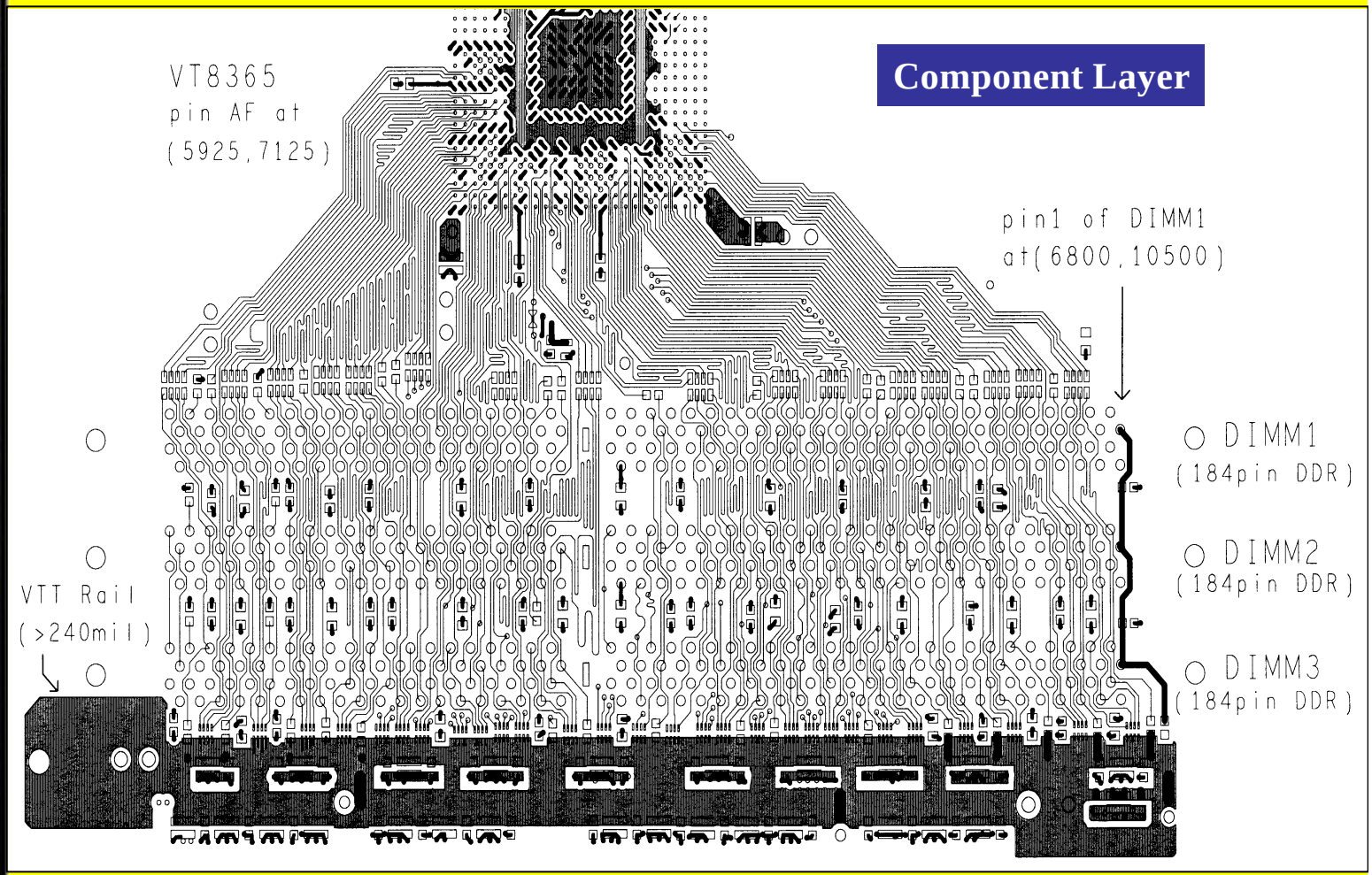
Summary

- **PRO266 and KT266 DDR chipsets both in volume production today:**
  - **Quality; Performance; Scalability**
  - **Enable DDR/SDR Transition**
  - **Serves as a baseline architecture for future VIA DDR SMA chipsets**
- **Supports ACR for a better connected PC platform**
  - **AMR compatible, audio, V.90.**
  - **Dual MII interfaces for Ethernet of Home PNA**
  - **Future DSL and Wireless communications**
- **DDR Promotion/Enabling Program**
  - **DDR Validation program is in place**
  - **DDR Summit Press Conference on Feb. 06**
  - **DDR Media Evaluation Rebate Program**

Back Up

Layout Example of 3 DDR w/o ECC



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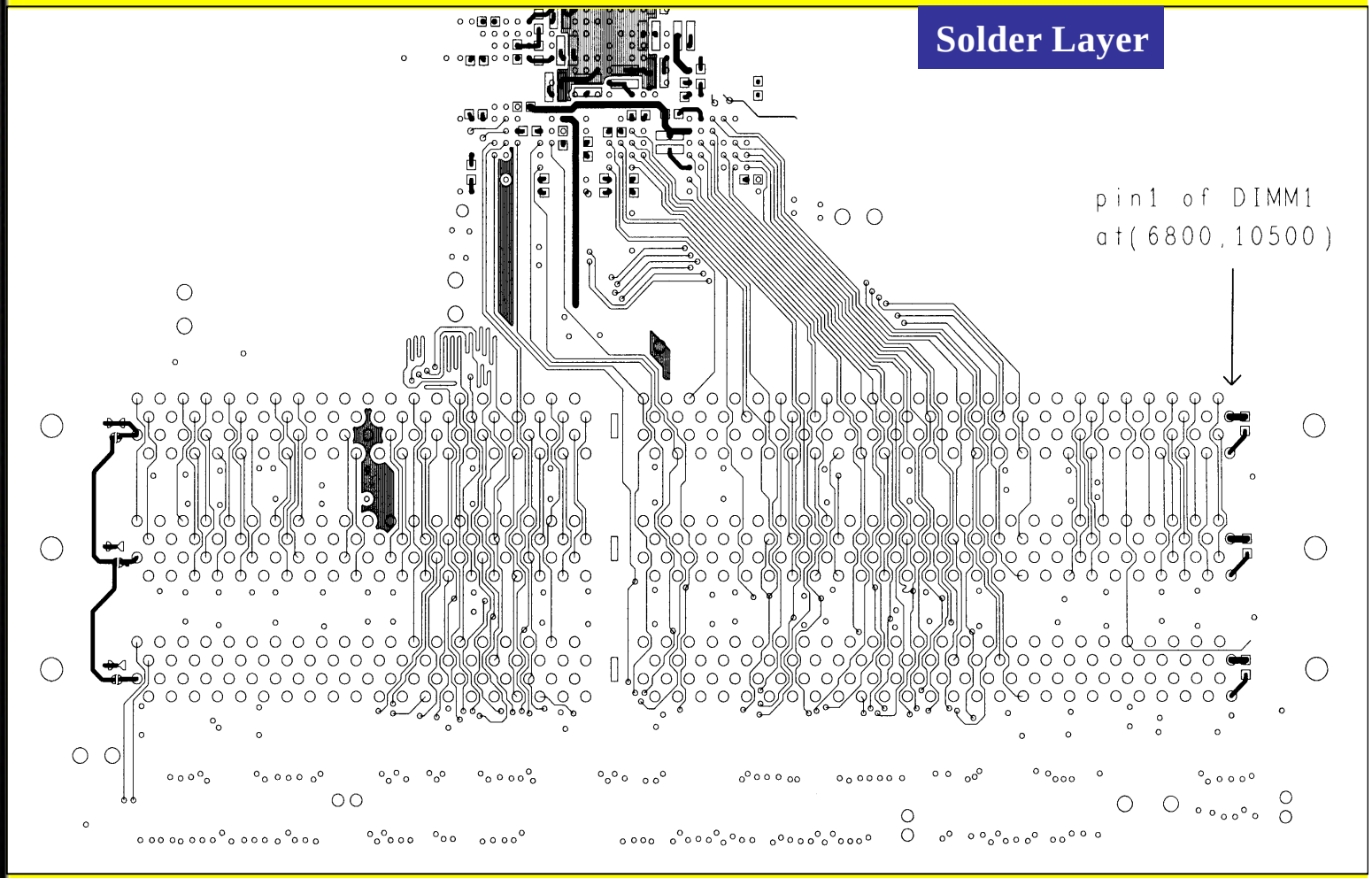
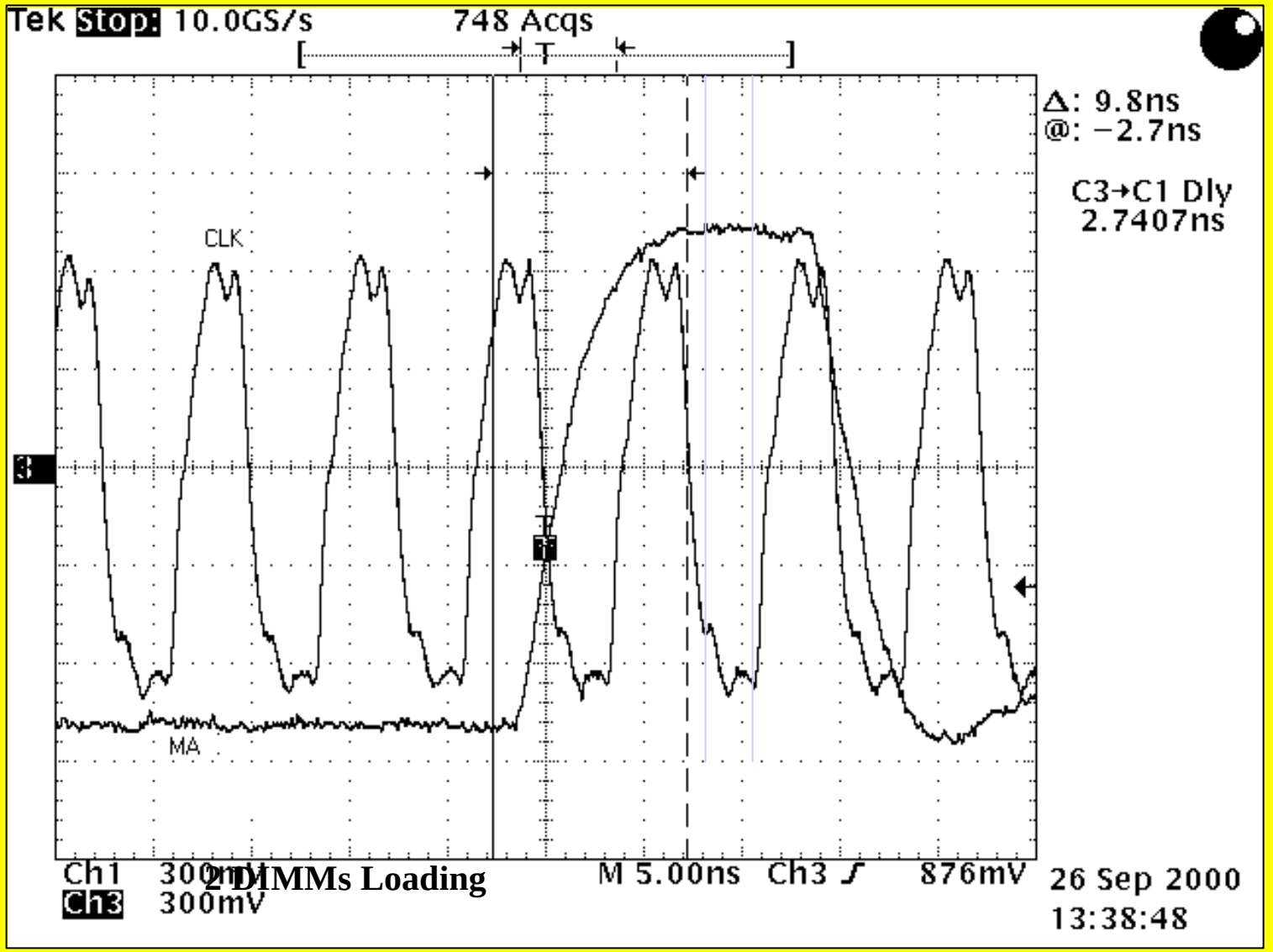
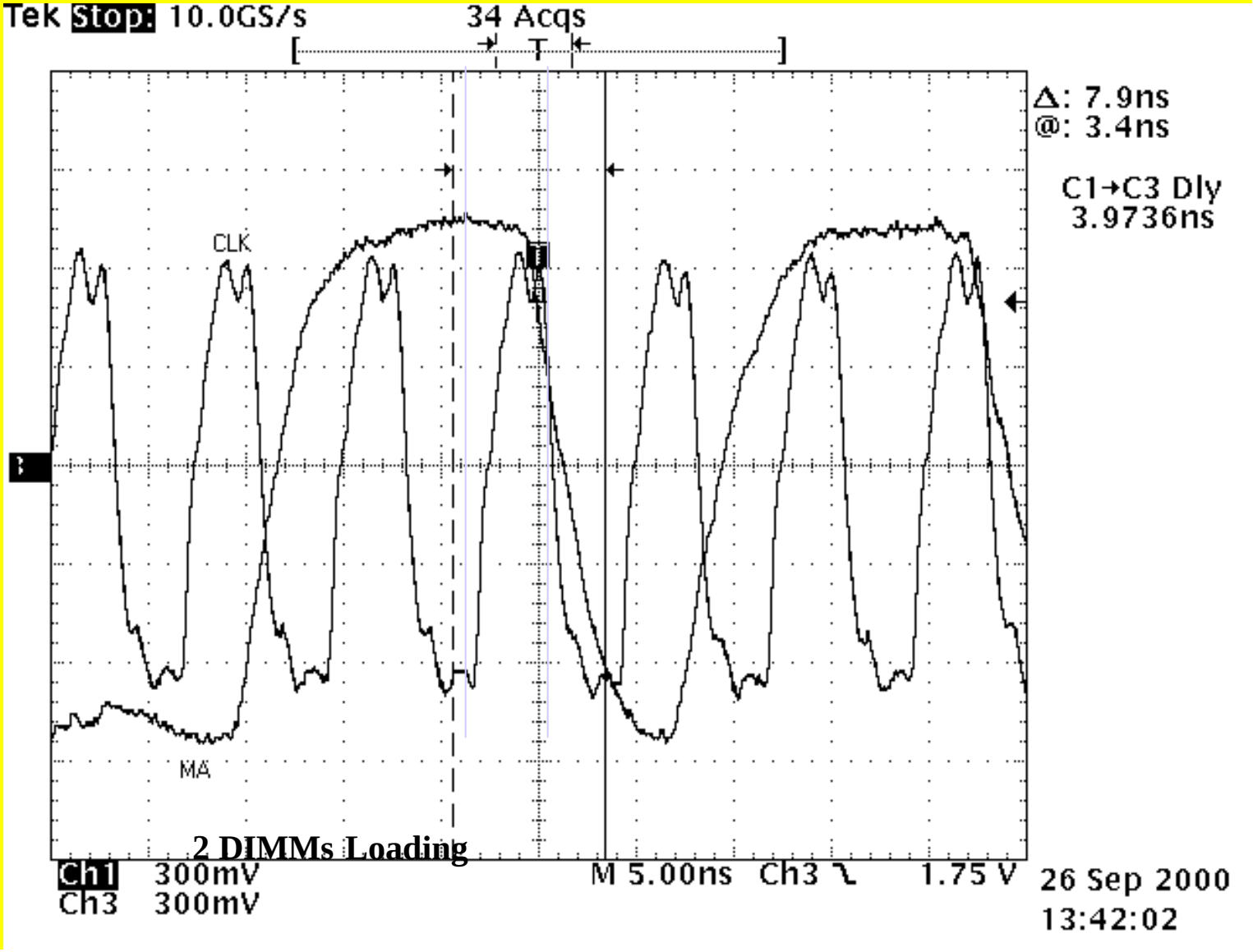


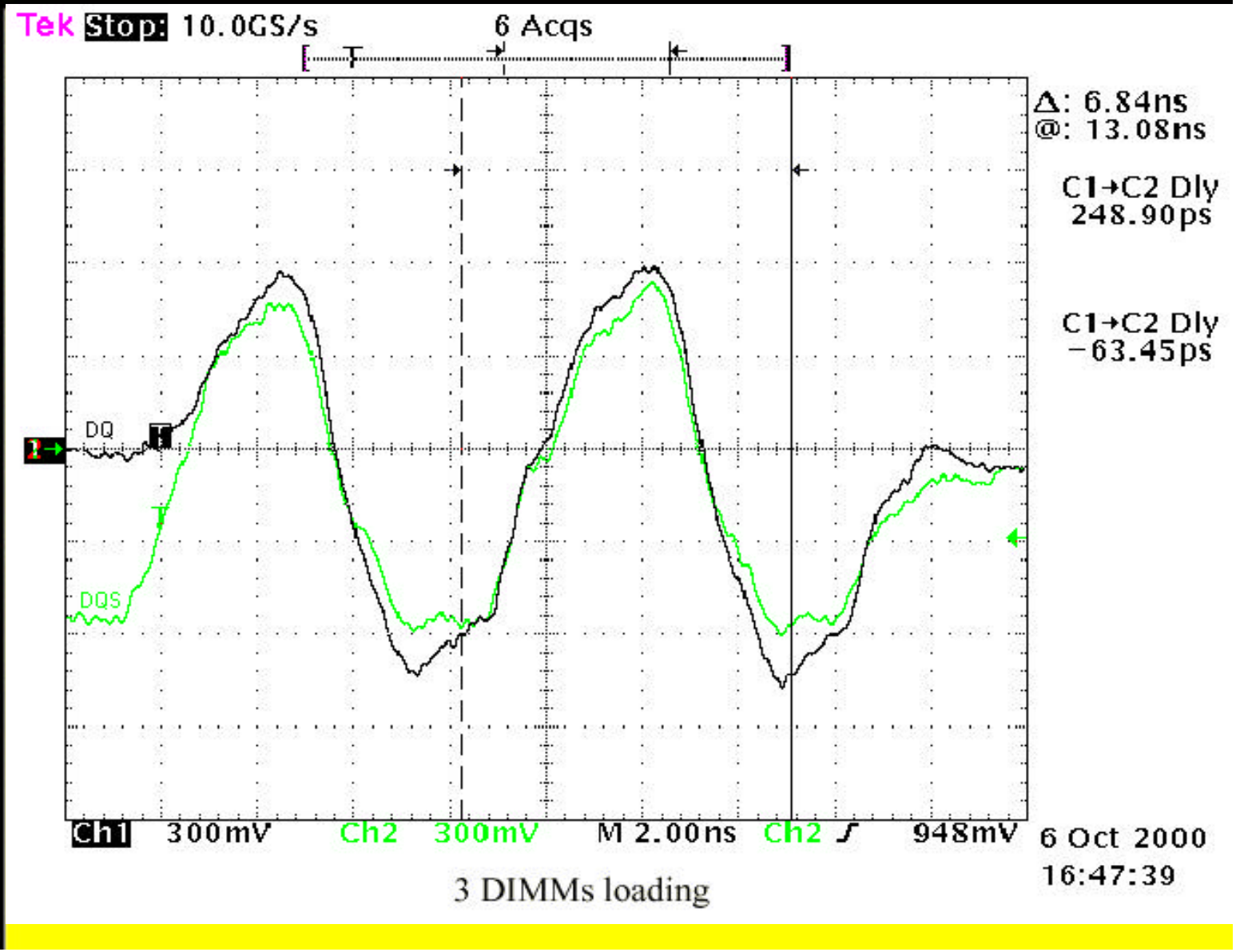
Waveforms: Add/CMD Setup



Waveforms: Add/CMD Hold



Waveforms/Read: DQ, DQS, DM



3 DIMMs loading

Vlink Layout Example (Top)